Claims

The following is a copy of Applicants' claims as currently pending in this application.

1. (Previously presented) A method for testing circuits having analog components, comprising:

performing a low-cost optimized test on the circuit by applying an optimized input stimulus to the circuit, the circuit having analog components;

capturing the circuit response to the input stimulus applied to the circuit;

evaluating the circuit response to predict whether the performance parameters of the circuit satisfies predetermined specifications for the circuit; and

making a pass/fail determination for the circuit based upon the evaluation of the circuit response.

2. (Original) The method of claim 1, wherein the low-cost optimized test is used to evaluate compliance with each specification specified for the circuit being tested.

3. (Original) The method of claim 1, wherein the low-cost optimized test is used to evaluate compliance with less than each specification specified for the circuit being tested.

4. (Previously presented) The method of claim 1, wherein the low-cost optimized test is designed to maximize the sensitivity of the circuit response to changes in circuit process parameters by deriving synthesizing functions which map measurement responses of the circuit to the circuit performance parameters.

5. (Original) The method of claim 1, further comprising performing specification based tests to circuits for which a clear pass/fail determination could not be made from the low-cost optimized test.

6. (Previously presented) The method of claim 5, wherein the specification based tests are applied to determine compliance with respect to less than all of the predetermined specifications for the circuit being tested.

7. (Previously presented) The method of claim 5, wherein the optimized test is created to minimize a variance, σ^2_{ei}, such that the number of specification based tests needed is minimized.

8. (Original) The method of claim 1, further comprising performing specification based tests to the circuits to determine compliance with one or more predetermined circuit specifications.

9. (Previously presented) The method of claim 8, wherein the specification based tests are applied to less than all of the predetermined circuit specifications specified for the circuit being tested.

10. (Previously presented) The method of claim 1, wherein the low-cost optimized test is formulated by deriving synthesizing functions which map a measurement response to circuit performance parameters.

11. (Original) The method of claim 10, wherein one synthesizing function is derived for each circuit specification to be tested.

12. (Previously presented) The method of claim 10, wherein the circuit response is input into the synthesizing functions to predict compliance with the predetermined specifications.

13. (Original) The method of claim 10, wherein the synthesizing functions are derived near the boundary of an acceptance boundary for each circuit performance parameter.

14. (Original) The method of claim 10, wherein the synthesizing functions are derived through nonlinear regression.

15. (Original) The method of claim 1, wherein the input stimulus is a sinusoidal stimulus.

16. (Original) The method of claim 1, wherein the input stimulus is derived using genetic algorithms.

17-28. (Cancelled)